Office of the Dean Research and Development

Indian Institute of Engineering Science & Technology (IIEST), Shibpur,

Howrah-711 103

Project Code: DRC/MNRE/CEGESS/HS/006/11-12

Centre of Excellence for Green Energy & Sensor Systems

Indian Institute of Engineering Science & Technology (IIEST), Shibpur

Howrah-711 103

Notice Inviting Quotations

Sealed quotations are invited for the supply of **Wafer** as per the following technical specification. The relevant technical specification can be downloaded from the website. The document can be also obtained from the Centre of Excellence for Green Energy & Sensor Systems (contact: Prof. H. Saha) between 10.30 a.m. and 3.00 p.m. on all working days. The invitation is valid for 7 working days from the date of publication of this notice.

Dean (R & D)

(A. Code DRC-T042/16-17)

SECTION I: TERMS & CONDITIONS

1. The last date of receipt of quotation is valid **for 7 Working days** from the date of publication of this notice. Quotations received later will not be entertained under any circumstances.

2. Potential supplier are to submit the quotations in Sealed Cover to the Centre of Excellence for Green Energy & Sensor Systems in the following address:

   Prof. Hiranmay Saha
   Chair Professor & Project Investigator
   CEGESS
   IIEST, Shibpur
   Howrah-711103, India

3. Item name must be mentioned on cover

4. The price quoted should be inclusive of all Taxes in INR, duties and levies. Inclusion of Tax/Levy at a latter stage will not be accepted. Freight, Insurance charges should be clearly indicated.

Specification for WAFER

1.Textured p-Type wafer with one side n-diffused prime Cz-mono Crystalline wafers

Doping surface Sheet resistance (n-layer) must be 80-100 ohm/sqr (with less than 5% tolerance)
Integrated reflection from the surface not greater than 10-12%
Lifetime of the Wafers must be greater than 100us.

Quantity : 200 nos.

2. Textured p-Type wafer with one side n-diffused silicon nitride coated on n-diffused prime Cz- mono Crystalline wafers

Doping surface Sheet resistance (n-layer) must be 80-100 ohm/sqr (with less than 5% tolerance)
Integrated reflection from the surface not greater than 4.5%
Lifetime of the Wafers must be greater than 100us.

Quantity : 200 nos.

All wafer size will be 6" x 6" pseudo square. Thickness will be 180um (with less than 5 um tolerance)