DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING

INDIAN INSTITUTE OF ENGINEERING SCIENCE AND TECHNOLOGY, SHIBPUR

HOWRAH-711103

CPDA Order No.: 2088/Dean(FA)/CPDA/17 **Dated: 03.03.2017**

Advt.No.Web/ETC/IIEST/16-17/130

Notice Inviting Quotations

Sealed quotations are invited for the supply of

(i) **SPARTAN 6 FPGA Trainer Kit**

as per the prescribed specifications. The relevant bidding document can be Downloaded from the website. Last date of submission of sealed quotation is 7 working days from the date of publication of the tender in the institute website.

This is downloadable

INDIAN INSTITUTE OF ENGINEERING SCIENCE AND TECHNOLOGY (IIEST) SHIBPUR

BIDDING DOCUMENT

For Supply of

(i) **SPARTAN 6 FPGA Trainer Kit**

Under

CPDA Fund

Department of Electronics and Telecommunication Engineering
March 03rd, 2017

SECTION I:
TERMS & CONDITIONS AND IMPORTANT INSTRUCTIONS FOR BIDDERS

1.Bidders are to invited to submit sealed quotation as per the technical specifications for tendered item to Dr. Ayan Banerjee, Associate Professor, Department of Electronics and Tele Communication Engineering, **on or before 10/03/2017** between **10.30 a.m. to 3.00 p.m**. except Saturday, Sunday and other public holidays.

2. The last date of receipt of tenders is **10/03/2017** up to **3.00 p.m.** quotations received later will not be entertained under any circumstances.

3. Date and time of opening of bid is **10/03/2017** at **04.00 p.m.** and the place of opening of bid is office of the H.O.D, Department of Electronics and Telecommunication Engineering, Indian Institute of Engineering Science and Technology (IIEST) Shibpur, Howrah-711103.

4. Bidders are to submit the quotations in Sealed Cover to the Department of Electronics and Telecommunication Engineering in the following address:

Dr. Ayan Banerjee
Associate Professor
Department of Electronics and Telecommunication Engineering
Indian Institute of Engineering Science and Technology
(IIEST) Shibpur
Howrah-711103, India

5. All bids should be submitted in ONE-BID (TECHNO-COMMERCIAL BID)
Format in covers (Enquiry Number must be mentioned on cover).

TECHNO-COMMERCIAL BID - giving Detailed Specifications, International Standards (BIS/INTERNATIONAL), Catalogues, List of users & Technical Details / Operating Parameters, Pre-Installation Requirements, payment terms, warranty, etc. along with PRICE BID - giving full Prices in Indian Rupees (only) for

(a) Tendered item.
(b) Essential Accessories & Spares.

6. The price quoted should be inclusive of all Taxes, duties and levies. Inclusion of Tax/Levy at a later stage will not be accepted. Freight, Insurance charges should be clearly indicated.

7. The materials are to be supplied at a place within IIEST premises between 11.00 a.m. and 4.00 p.m. The tendered will be responsible for any breakage, damage or defect in the equipment detected subsequently. The supply and installation of the equipment should be completed within a period not exceeding 3 months from the placement of the formal work order or opening of the LC failing which appropriate action will be taken as per Institute rules.

8. If the supply is not completed within the stipulated period as indicated in the Work Order, a Liquidated Damage @ ½ per cent per week will be imposed subject to maximum of 5% of the value of work order.

9. For Indian purchase (*This clause is applicable only for Indian purchase and not applicable for foreign purchase*):
Bill should be presented for payment within 10 days of Supply / Completion of work. No Advance Payment can be made. All bills are to be accompanied by Order copies and Challan Receipt. The Order Number is to be noted on both the Challan and the Bill.

10. Documents to be submitted with the tender:
Tender Documents/Terms & Conditions in Original duly signed by the Proprietor / Partner/ Director of the Company as a token of acceptance of Terms & Conditions of Tender.

11. Customs Duty & Excise Duty
 The Institute will not issue any C or D form availing of concessional Sales Tax/ VAT.
 The Institute will issue Customs Duty Exemption Certificate or Excise Duty Exemption Certificate for foreign purchase, if required.

12. Indian Institute of Engineering Science and Technology (IIEST) Shibpur, Howrah reserves the right to accept / reject all or any of the tenders without assigning any reason whatsoever.

We accept the above terms and conditions.

Dated: Signature of Bidders/Suppliers
With date & Seal

SECTION II: <u>TECHNICAL SPECIFICATIONS</u>

Sl. No	ITEM	QUANTITY
01	**<u>SPARTAN6 FPGA Trainer Kit</u>** • Baseboard &XLINIX XC6SLX4TQ144:SPARTAN6 FPGA Daughter Board. • JTAG Cable(JTAG port or Serial port of the daughter board on one end and to PC parallel port on the other end), Converters/Connectors.	3 Nos (Sets)

- Programming tool & Power supply.

BASE BOARD Specification

- ✓ 32 Toggle switches for I/P selection with 32 LEDs to indicate switch status.
- ✓ 32 LEDs connected to output ports of the FPGA.
- ✓ 2 line X 16 Alpha-Numeric LCD display with back-light.
- ✓ Four digit 7-segment display.
- ✓ 4 X 4 key matrix.
- ✓ 2 nos. of Push button switches.
- ✓ On board 10 MHz oscillator.
- ✓ 10 MHz clock and one of four different frequency clocks (5Mhz, 1Mhz, 500Khz and 100Khz).
- ✓ User I/Os available for Pattern generator and Logic Analyzer connection.
- ✓ On-board different supply voltage generator to match the multi-volt with LED indication.
- ✓ Support for different FPGA/CPLD of different makes (1.8V, 2.5V, 3.3V, 5V) with LEDs to identify the card type.
- ✓ 26-pin FRC connector for connecting to ALS standard interface boards like Stepper motor, ADC, DAC, Traffic light controller, Elevator, Printer interface etc.
- ✓ Four sets of 20 X 2 female berg connectors to plug the child card.
- ✓ Standard VGA interface through 9-PIN D-type connector.
- ✓ PS/2 standard external keyboard/mouse interface.
- ✓ RS232 serial interface through 9-PIN D-type connector.

DAUGHTER BOARD Specification

- ✓ XLINIX XC6SLX4TQ144: SPARTAN6 FPGA.
- ✓ Built on mature 45nm low-power copper process technology.
- ✓ Provision for on-board PROM for storing FPGA configuration bit stream(Platform flash in-system programmable configuration PROM: XCF04SVO20).
- ✓ 500K System gates, 3840 logical cells,4800 flip-flops.
- ✓ 75K distributed RAM.
- ✓ 18 Kb (2 x 9 Kb) block RAMs/ 126KB block RAM.
- ✓ Second generation DSP48A1 slices.
- ✓ LX4TQG144 pin package with 102 I/O lines.
- ✓ I/O tolerant 3.3V.
- ✓ IC with JTAG Connector for Boundary Scan programming.
- ✓ 16 PIN FRC connector to select between base board toggle switch and the 26 pin FRC external interface.
- ✓ JTAG connector (10 PIN FRC connector) for boundary scan programming.
- ✓ Push-button switch to re-initialize the FPGA and DONE LED for program status indication.
- ✓ Power from the bottom base board.
- ✓ Four sets of 20 X 2 berg connectors for plugging on to the base board.