



# IEST, Shibpur

Indian Institute of Engineering Science and Technology, Shibpur  
(Formerly Bengal Engineering and Science University, Shibpur)

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## *Personal Information*

**Name:**Dr.SudipGhosh.

**Designation:**Assistant Professor, School of VLSI Technology, IEST Shibpur.



## **Academic Qualifications:**

1. Ph.D. (Engineering), Indian Institute of Engineering Science and Technology, Shibpur (IESTS), 2017.
  2. M.S. (VLSI CAD), 2005
  3. B.E. (Electronics & Communication Engineering), 2001
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## *Contact Information*

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## *Area of Research*

1. FPGA and SoC based Digital Watermarking Architectures.
  2. Synthesis and Verification of Digital circuits.
  3. VLSI Testing.
  4. Advanced Computer Architectures.
  5. Image and Video signal processing hardware architectures.
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## *Courses Undertaken*

### **PG Courses**

1. VLSI Testing (VLSI-903)

2. Advanced System Architecture (VLSI-904/1)
3. Synthesis and Verification Techniques (VLSI-1004)
4. SoC and Memory Design and Test (VLSI-1150/2)
5. Digital Signal Processing (VLSI-905/2)

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## Recent Publications

### CONFERENCES

2006

[1] Nachiketa Das, SudipGhosh and H.Rahaman. "Detection of Single Stuck-at and Bridging Faults in Cluster Based FPGA architectures", in IEE national seminar EEDP-2006 on 12th March, 2006 at JIS College of Engineering, Kalyani, West Bengal, India.

2007

[2] SomsubhraTalapatra, SudipGhosh, C.Roychaudhuri, Biplab K. Sikdar and HafizurRahaman. "FPGA based Design and Implementation of Neural Network Compensators for Nanocrystalline MEMS pressure sensor" in VSI, TEQIP, DIT sponsored national conference on Design Techniques for modern electronic devices, VLSI and Communication Systems (DTVC- 2007) from 14th -15th May, 2007 at NIT Hamirpur ,Himachal Pradesh, India. pp. 183-188.

url: <http://vlsi-india.org/vsi/photos/2007/dtvc07/index.html>

[3] Nachiketa Das, SudipGhosh and H.Rahaman. "Detection of Single Stuck-at and Bridging Faults in Cluster-based FPGA Architectures" in 11th IEEE International Symposium on VLSI Design and Test (VDAT- 2007) from 8th –11th August, 2007 at Saha Institute of Nuclear Physics (SINP), Kolkata, India. pp. 205-212.

url: <http://vlsi-india.org/vsi/download/vdat-abs/vdat2007-abstract.pdf>

2009

[4] SudipGhosh, Pranab Ray, Santi P Maity and HafizurRahaman "Spread Spectrum Image Watermarking with Digital Design" in IEEE International Advance Computing Conference(IACC 2009) from 6-7 March 2009 at Thapar University, Patiala, India. pp. 868 – 873.

url: <http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=4809129>

2010

[5] SudipGhosh, SomsubhraTalapatra, Santi P Maity and HafizurRahaman "A Novel VLSI Architecture for Walsh-Hadamard Transform" in IEEE 2nd Asia Symposium on Quality Electronic Design (ASQED-2010) from 3-4 August, 2010 at Penang, Malaysia. pp. 146 – 150.

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2012

[6] SudipGhosh, SomsubhraTalapatra, DebasishMondal, NavonilChatterjee, HafizurRahaman and Santi P Maity, “VLSI Architecture for Spatial Domain Spread Spectrum Image Watermarking using Gray-Scale Watermark”, in *16th International Symposium on VLSI Design and Test (VDAT, 2012)* from 1-4 July 2012 at Bengal Engineering and Science University, Shibpur, India. pp. 375-376. (Springer, LNCS)

Url: [http://dx.doi.org/10.1007/978-3-642-31494-0\\_49](http://dx.doi.org/10.1007/978-3-642-31494-0_49)

[7] SudipGhosh, SomsubhraTalapatra, DebasishMondal, NavonilChatterjee, HafizurRahaman and Santi P Maity, “VLSI Architecture for Spread Spectrum Image Watermarking using BinaryWatermark” in *IEEE, International Conference on Advances in Computing and Communications(ICACC)*, from 9-11August 2012 at Rajagiri School of Engineering & Technology, Cochin, Kerala, India 2012. pp. 166 - 169.

url: <http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6305580>

[8] SudipGhosh, SomsubhraTalapatra, Jayasree Sharma, NavonilChatterjee, HafizurRahaman and Santi P Maity, “Dual Mode VLSI Architecture for Spread Spectrum Image Watermarking using Binary Watermark” in *2nd International Conference on Communication, Computing & Security (ICCCS-2012)* from 6-8 October 2012 at National Institute of Technology Rourkela, India. pp. 784-791.

url: <http://dx.doi.org/10.1016/j.protcy.2012.10.095>

[9] SudipGhosh, SomsubhraTalapatra, SudiptaChakraborty, NavonilChatterjee, HafizurRahaman and Santi P Maity, “VLSI Architecture for Spread Spectrum Image Watermarking in Walsh-Hadamard Transform Domain using Binary Watermark” in *3rd IEEE International Conference on Computer and Communication Technology ( ICCCT 2012)* from 23-25 November 2012, at Motilal Nehru National Institute of Technology(MNNIT), Allahabad, India, pp. 233-238.

url: <http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6394703>

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[10] SudipGhosh, SomsubhraTalapatra, NavonilChatterjee, Nagakumar Reddy, Santi P Maity and HafizurRahaman, “Multiplier-less VLSI Architecture of 1-D HilbertTransform pair using Biorthogonal Wavelets” in *2nd IEEE International Conference of Informatics, Electronics & Vision (ICIEV 2013)* from 17-18 May 2013, at University of Dhaka, Bangladesh. pp. 1 - 6.

url: <http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6572716>

[11] SudipGhosh, Santi P. Maity and HafizurRahaman, “Multiplier-less VLSI Architecture of 1-D Hilbert Transform pair using Biorthogonal Wavelets for QCM-SS image Watermarking”, in *4th IEEE International Conference on Computer and Communication Technology (ICCCT- 2013 )* from 20th -22nd September 2013, at Motilal Nehru National Institute of Technology(MNNIT), Allahabad, India. pp. 5-10.

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[12] SudipGhosh, BijoyKundu, DebopamDatta, Santi P Maity and HafizurRahaman “Design and Implementation of Fast FPGA based Architecture for Reversible Watermarking” in *IEEE International*

*Conference on Electrical Information and Communication Technology (EICT-2013) from 19-21 December 2013, at Khulna University of Engineering and Technology (KUET), Khulna, Bangladesh. pp.1-6.*

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2014

*[13] SudipGhosh, ArijitBiswas, Santi P Maity and HafizurRahaman "Hadamard Walsh and Paley Ordered DFWHT: A Study and Implementation on FPGA" in IEEE CALCON 2014 National Conference on Electrical, Electronics, and Computer Engineering (A Triennial Event of IEEE Kolkata Section) from November 7-8, 2014 at Hotel Park Prime Kolkata,India , ISBN 978-93-833-0383-0*

*[14] SudipGhosh, Nachiketa Das, SubhajitDas,Santi P Maity and HafizurRahaman "FPGA and SoC Based VLSI Architecture of Reversible Watermarking Using Rhombus Interpolation By Difference Expansion" in 11th IEEE India Conference INDICON 2014 from 11th to 13th December 2014 at Yashada,Pune,India. pp. 1-6.*

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*[15] SudipGhosh, ArijitBiswas,Santi P Maity and HafizurRahaman "Design of A Low Complexity and Fast Hardware Architecture for Digital Image Watermarking in FWHT Domain on FPGA" in 5th IEEE International Symposium on Electronic System Design (ISED 2014) from December 15 - 17, 2014 at NIT Surathkal, Mangalore,India. pp. 68-72.*

*url: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7172749>*

*[16] SudipGhosh, ArijitBiswas, Santi P Maity and HafizurRahaman "Design of an Improved Algorithm for Blind Digital Image Watermarking Using Both Grayscale and Binary Watermark in DFWHT Domain" in 8th IEEE International Conference on Electrical and Computer Engineering (ICECE 2014) from 20-22 December 2014 at Pan Pacific Sonargaon,Dhaka, Bangladesh. pp. 112-115.*

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*[17] SudipGhosh, Nachiketa Das, SubhajitDas,Santi P Maity and HafizurRahaman "Digital Design and Pipelined Architecture for Reversible Watermarking Based on Difference Expansion using FPGA" in 13th IEEE International Conference on Information Technology (ICIT 2014) from 22nd -24th December, 2014 at Bhubaneswar,Orrisa, India. pp. 123-128.*

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2015

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[21] SudipGhosh, SambaranHazra, Santi P Maity and HafizurRahaman "A New Algorithm for Grayscale Image Histogram Computation" in *12th IEEE India International Conference (INDICON) 2015 from 17-20 December 2015 at JamiaMilliaIslamia, New Delhi, India.* pp. 1-6.

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## 2016

[22] Subrata Das., ParthasarathiDasgupta, PetrFiser, SudipGhosh and Debesh Kumar Das "A Rule-Based Approach for Minimizing Power Dissipation of Digital Circuits" in *19th IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS) from April 20-22, 2016, at Košice, Slovakia, Europe.* pp. 1-6.

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[23] SambaranHazra, SudipGhosh, Santi P. Maity, HafizurRahaman "New FPGA and Programmable SoC Based VLSI Architecture for Histogram Generation of Grayscale Images for Image Processing Applications" in *6th International Conference On Advances In Computing & Communications, ICACC 2016, 6-8 September 2016, Cochin, India.* vol. 93, Pp. 139–145.

url : <http://dx.doi.org/10.1016/j.procs.2016.07.193>

## JOURNALS

### 2012

[1] SudipGhosh, SomsubhraTalapatra, NavonilChatterjee, Santi P Maity and HafizurRahaman, "FPGA based Implementation of Embedding and Decoding Architecture for Binary Watermark by Spread Spectrum Scheme in Spatial Domain" in *Bonfring International Journal of Advances in Image Processing, Vol. 2, No. 4, December 2012.* pp. 01-08.

url: <http://www.journal.bonfring.org/abstract.php?id=1&archiveid=309>

2015

[2] *Sudip Ghosh, Arijit Biswas, Santi Prasad Maity and Hafizur Rahaman "Field Programmable Gate Array and System-on-Chip Based Implementation of Discrete Fast Walsh-Hadamard Transform Domain Image Watermarking Architecture For Real-Time Applications" in special issue of "Journal of Low Power Electronics" published by American Scientific Publishers in Vol. 11, No. 3, pp. 375-386, September 2015. doi: <http://dx.doi.org/10.1166/jolpe.2015.1388>*

2017

[3] *Sambaran Hazra, Sudip Ghosh, Sayandip De and Hafizur Rahaman "FPGA implementation of semi-fragile reversible watermarking by histogram bin shifting in real time" in special issue of Springer journal of Real-Time Image Processing, pp 1-29, online from 22nd February 2017. doi : [10.1007/s11554-017-0672-9](https://doi.org/10.1007/s11554-017-0672-9)*

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